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ANALYSIS OF TRANSISTOR AND SNUBBER TURN-OFF DYNAMICS IN HIGH-FREQUENCY HIGH-VOLTAGE HIGH-POWER CONVERTERS

Paul M. Wilson, Thomas G. Wilson, and Harry A. Owen, Jr.

Department of Electrical Engineering
Duke University, Durham, N.C., 27706 U.S.A.
Tel. 919-684-3123

The United States National Aeronautics and Space Administration has forseen a need for light-weight highly-efficient power-processing systems capable of providing regulated high-voltage outputs to loads which will eventually range into the hundreds of kilowatts. One of the key ingredients in the process of attaining this goal is the ability to design dc-to-dc converters which will operate reliably and efficiently at switching frequencies high enough to effect substantial reductions in the size and weight of the converter energy-storage elements. To date, research efforts have focused on the development of a two-winding current-or-voltage step-up (buck-boost) dc-to-dc converter power-stage submodule designed to operate in the 2.5-kW range, with an input-voltage range of 110 to 180 V dc, and an output voltage of 250 V dc. In order to assess the limitations of present-day component and circuit technologies, a design-goal switching frequency of 100 kHz has been maintained throughout the course of this research.

The above converter design requirements represent a unique combination of high-frequency, high-voltage, and high-power operation. The efficient and reliable operation of the converter power-semiconductor switches in such an environment represent a complex and formidable design problem. It is a portion of this problem which will be addressed by this paper; namely, the turn-OFF dynamics of the primary-circuit power switching transistor and its its associated turn-OFF snubber circuitry.

In such a high-frequency high-voltage high-power dc-to-dc converter, efficiency and reliability considerations mandate that the power transistor must switch large currents very quickly at transistor turn-OFF. Presently-available power semiconductor technology includes both bipolar junction transistors (BJTs) and metal-oxide-semiconductor field effect transistors (MOSFETs) capable of performing this task, with resulting circuit time rates of change of current di/dt ranging from 100 to 1000 A/μsec . The effects on the power switching transistor of these extremely high time rates of change of current, acting in conjunction with parasitic inductances in the converter principal power-flow paths, such as transformer leakage inductance and stray circuit-loop inductances, have been reported [1] [2] . Of primary concern is the transistor voltage overshoot at turn-OFF, which is excess of the transistor steady-state OFF voltage, and which results from the presence of parasitic inductance. Even with only modest amounts of parasitic inductance present in the converter circuit -- several hundred nanohenries, for instance -- the magnitude of the voltage overshoot can reach several hundred volts, potentially

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resulting in transistor failure from excessive voltage stress. This problem is particularly important from the standpoint of the present circuit application, where to some degree, transistor breakdown-voltage capability must be sacrificed to obtain devices with either the prerequisite switching speeds in the case of BJTs, or to obtain devices with sufficiently low ON-resistances in the case of MOSFETs. The answer to this problem lies in the ability to design circuitry which limits the magnitude of the transistor voltage overshoot at turn-OFF to a value commensurate with the breakdown-voltage rating of currently-available transistors.

Of the potential candidate circuits available for performing this function, the network which appears to be the most promising in light of the present application is the LC-type snubber, depicted in conjunction with the two-winding energy-storage-reactor current-or-voltage step-up converter in Fig. 1. In addition to performing the important task of controlling the transistor voltage overshoot at turn-OFF, the LC-type snubber also performs another equally important function -- that of shaping the transistor turn-OFF trajectory. This second function is important from the standpoint that power dissipation within the transistor Q at turn-OFF is reduced through the action of the snubber. In addition, by making use of this waveshaping action of the LC-type snubber, the snubber can be designed so as to contain the transistor turn-OFF switching trajectory to within the boundaries imposed by the reverse-bias safe operating area (RBSOA) of a BJT. Naturally, how well the LC-type snubber actually performs these critical functions in a high-frequency high-voltage high-power environment is of paramount importance.

Figure 2 is an equivalent circuit diagram of the two-winding current-or-voltage step-up converter and LC-type snubber, along with a number of various discrete parasitic inductances, shown as dashed circuit elements L_1 through L_5, which are of importance in determining the dynamic behavior of the transistor and snubber circuit at turn-OFF. The inductances L_1 through L_5 represent in a discrete manner the distributed parasitic inductances associated with either:

(1) a component, such as the equivalent series inductance (ESL) of a capacitor, or the leakage inductance of the two-winding energy-storage reactor X; or

(2) circuit geometry, i.e., the distributed inductance associated with a circuit loop; or

(3) a combination of both (1) and (2) above.

In particular, L_1 represents the sum total, referred to the primary circuit, of the combination of transformer leakage inductance and all secondary-circuit parasitic inductances, and is normally the largest of the parasitic inductances under consideration. L_2 represents the geometry-dependent distributed inductances associated with the circuit loop composed of Q, C_S, D_{S1}, and C_{IN}. L_3 and L_4 represent the ESLs of C_{IN} and C_S, respectively, and L_5 represents the inductive behavior of the snubber diode D_{S1} during its turn-ON transient.

In many circumstances, where extremely fast transistor turn-OFF switching performance is not as critical as in the present application, and therefore circuit time rates of change of current need not be so very high, the effects of the inductances L_2 through L_5 may be so small as to be almost negligible.

An analysis has been presented for the case where the effects of the inductances L_2 through L_5 are neglected [3], and transistor current and voltage waveforms for the transistor turn-OFF interval corresponding to such an analysis are depicted in Fig. 3(a). In Fig. 3(b), oscillograms of transistor current i_Q and voltage v_Q during the turn-OFF interval are shown for an experimental two-winding current-or-voltage step-up converter power stage with an LC-type snubber operating at an output-power level of approximately 500 W, and at a switching frequency of 100 kHz. It is the disparity between the shapes of the two sets of waveforms in Figs. 3 (a) and (b) that motivates the modeling and analysis to be presented in this paper, an analysis which in part will deal with the effects of the inductances L_2 through L_5 on the dynamic behavior of the transistor turn-OFF waveshapes. Figure 4 further illustrates the effect of inductances L_2 through L_5, where the transistor turn-OFF switching trajectory in the i_Q versus v_Q plane is shown for three cases. In the first case, the turn-OFF trajectory (A) is shown for the condition where the effects of the inductances L_2 through L5 are assumed to be negligible. In the second case, the turn-OFF trajectory (B) includes the effects of L_2 through L_5. Finally, the third turn-OFF trajectory (C) corresponds to the case where significant parasitic inductance is present, but no turn-OFF snubber is used. For reference, a dashed curve depicting a shape representative of a typical BJT RBSOA is also shown. It can be seen from Fig. 4 that when a more realistic model including the effects of inductances L_2 through L_5 is employed, the turn-OFF switching trajectory begins to resemble the case where no snubber is used, with subsequently higher predicted transistor turn-OFF power dissipation, accompanied by the potential for violating the restrictions imposed by the boundaries of the RBSOA for the case where a BJT is used for the primary circuit power switch.

In addition to analyzing the effects of various circuit parasitic inductances on the transistor turn-OFF switching trajectory, this paper will also examine the effects of the reverse-recovery transients associated with snubber diodes D_{S1} and D_{S2}, particularly as these reverse-recovery transients, in conjunction with parasitic inductance, affect the waveforms associated with the power switching transistor, and as they affect the operation of the LC-type snubber.

To summarize, the nonideal nature of various converter-circuit and snubber-circuit components, in addition to circuit-layout-related effects, have a profound influence on the dynamic behavior of the power switching transistor at turn-OFF, particularly in a high-frequency high-voltage high-power environment. The purpose of this paper will be to extend the analysis of the turn-OFF behavior of a power switching transistor, operating in conjunction with an LC-type turn-OFF snubber, to include the effects of those parasitic circuit elements necessary to accurately portray the transistor turn-OFF switching trajectory, allowing a more accurate portrait of the losses associated with the transistor and snubber circuitry.

REFERENCES:

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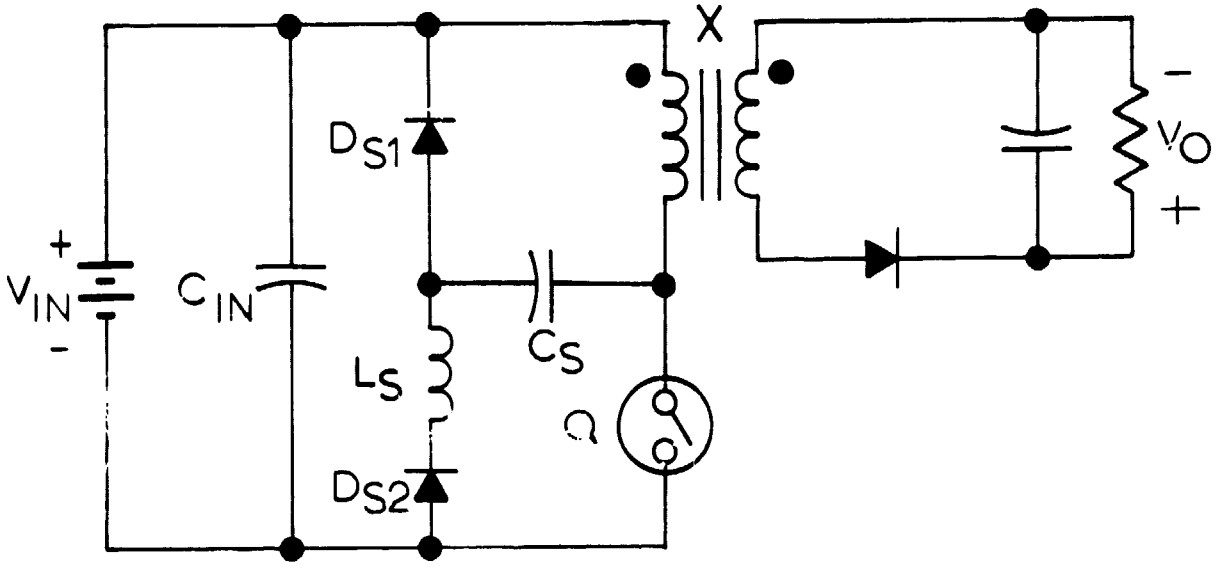

Fig. 1. Schematic diagram of two-winding current-or-voltage step-up converter power stage with LC-type snubber.

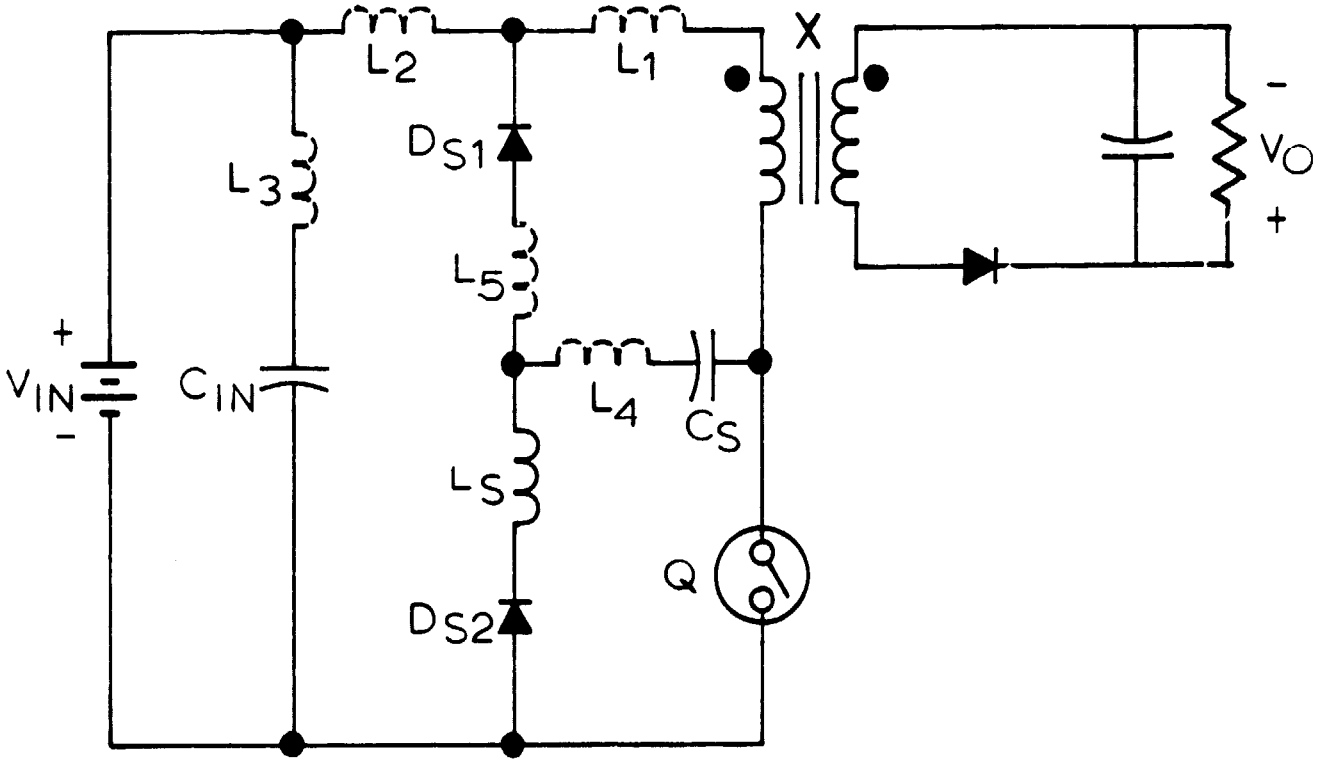

Fig. 2. Equivalent circuit diagram of converter power stage with LC-type snubber indicating locations of parasitic inductances L_1 through L_5 (shown as dashed circuit elements).

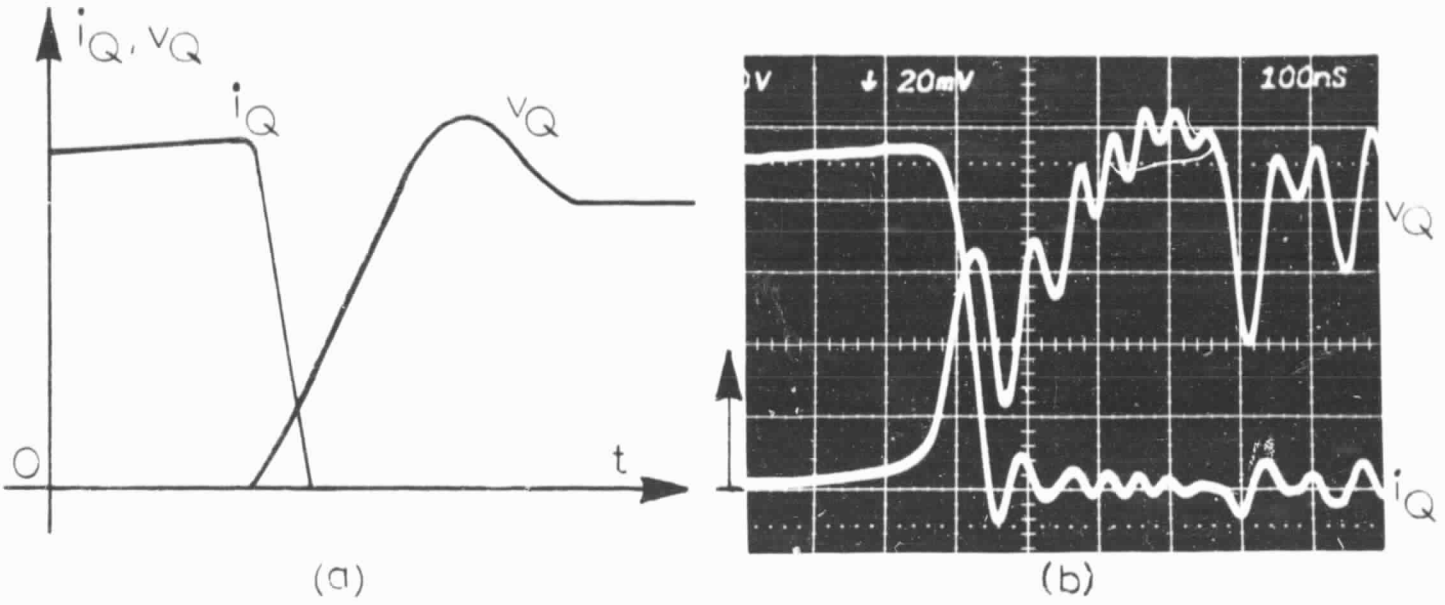

Fig. 3. (a) Transistor current i_Q and voltage v_Q waveforms predicted by circuit analysis in which the effects of inductances L_2 through L_5 are neglected. (b) Oscillogram of transistor current i_Q and voltage v_Q taken from experimental current-or-voltage step-up converter. Scale factors are: i_Q, 4 A/div.; v_Q, 50 V/div.; and time, 100 ns/div.

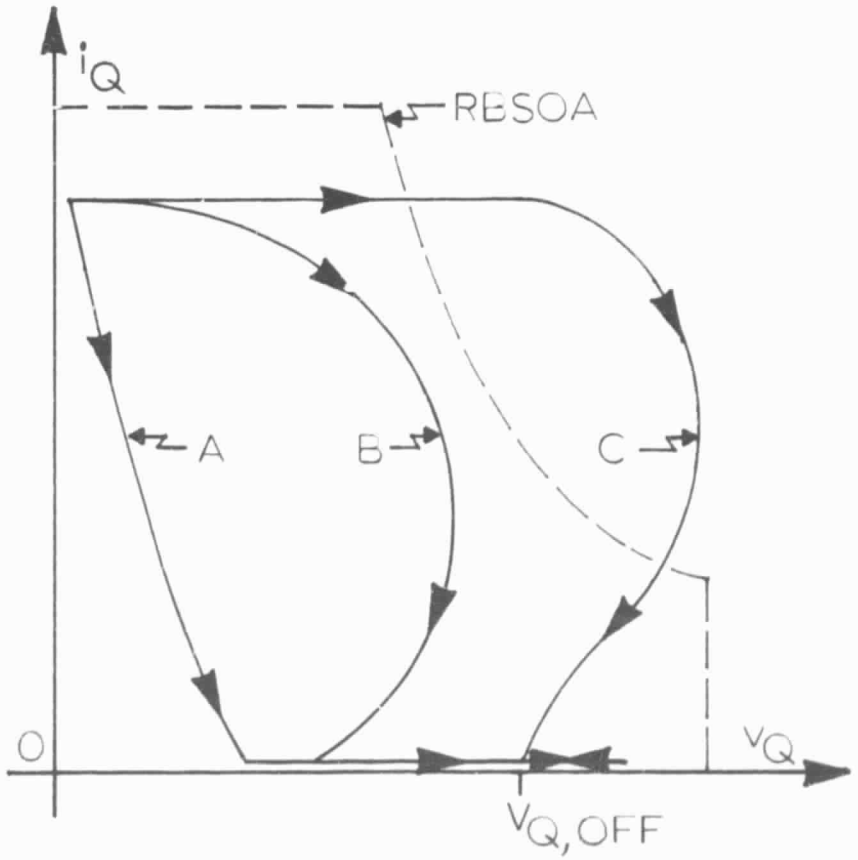

Fig. 4. Transistor turn-OFF switching trajectories as predicted by circuit analysis in which the effects of inductances L_2 through L_5 are neglected (curve A), and in which the effects of L_2 through L_5 are included (curve B). Also shown is the switching trajectory for operation without a snubber (curve C), and a curve representative of a typical BJT RBSOA (dashed curve).